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5	BRS	L6	0	(slack adj value\$3) same (fanins)	US-PGPUB	2006/12/30 10:42
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... The **slack** available to a node ... first compute the set of all nodes which feed primary outputs with **negative slack**. ... The set, Preds, of fanins of is first computed ...

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L Benini, G De Micheli, A Liou, E Macii, G Odasso, ... - [ieeexplore.ieee.org](#)

... The **slack**,  $ST_g; x$ , of a gate  $g$  is the difference between its required time and its arrival time, ie,  $ST_g; x = RT_g; x - AT_g; x$ . A path in a ...

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... Again, critical arcs are those arcs having the most **negative slack**, where **slack** is now defined for the early signals, as in equations (9) and (10) with ...

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... Then, it finds a **slack** for each node. Finally, from primary outputs, it assigns high-V<sub>t</sub> logic cells to nodes if it does not cause any **negative slack**. ...

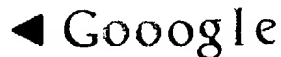
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5	BRS	L5	0	(slack same reduction same fanis)	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	2006/12/30 10:13

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9	BRS	L9	0	(slack same (value values)) and (time\$4 same delays) and fanis	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	2006/12/30 10:07
10	BRS	L10	5	(slack same (value values)) and (time\$4 same delays) and fanins	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	2006/12/30 10:07

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12	BRS	L12	0	(slack same reduction same fanins)	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWEN T; IBM_TDB	2006/12/30 10:13

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Instead, [17] distributes the pre-union SPFDs to its fanins. In their ... final average **delay reduction** is 5.8% by SPFD-ER and 2.6% by. SPFD-LR. ... [portal.acm.org/ft\\_gateway.cfm?id=774671&type=pdf](http://portal.acm.org/ft_gateway.cfm?id=774671&type=pdf) - [Similar pages](#)

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### 1 [Monotone bipartitioning problem in a planar point set with applications to VLSI](#)


 Parthasarathi Dasgupta, Peichen Pan, Subhas C. Nandy, Bhargab B. Bhattacharya  
 April 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,  
 Volume 7 Issue 2

Publisher: ACM Press

 Full text available: [pdf\(227.93 KB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A new problem called monotone bipartitioning of a planar point set is identified which is found to be useful in VLSI layout design. Let  $F$  denote a rectangular floor containing a set  $A$  of  $n$  points. The portion of a straight line formed by two points from the set  $A$  is called a line segment. A *monotone increasing path (MP)* in  $F$  is a connected and ordered sequence of line segments from the bottom-left corner of  $F$  to its top-right corner, such t ...

**Keywords:** Complexity of algorithms, floorplanning, partitioning, routing, very large scale integration (VLSI)

### 2 [A new enhanced SPFD rewiring algorithm](#)


 Jason Cong, Joey Y. Lin, Wangning Long  
 November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

 Full text available: [pdf\(567.60 KB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents an in-depth study of the theory and algorithms for the SPFD-based (*Set of Pairs of Functions to be Distinguished*) rewiring, and explores the flexibility in the SPFD computation. Our contributions are in the following two areas: (1) We present a theorem and a related algorithm for more precise characterization of feasible SPFD-based rewiring. Extensive experimental results show that for LUT-based FPGAs, the rewiring ability of our new algorithm is 70% high ...

### 3 [A novel net weighting algorithm for timing-driven placement](#)


 Tim (Tianming) Kong  
 November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**


Publisher: ACM Press

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Full text available:  pdf(119.90 KB)[terms](#)


Net weighting for timing-driven placement has been very popular in industry and academia. It has various advantages such as low complexity, high flexibility and ease of implementation. Existing net weighting algorithms, however, are often *ad-hoc*. There is generally no known *good* net weighting algorithms. In this paper, we present a novel net weighting algorithm based on the concept of path-counting, and apply it in timing-driven FPGA placement application. Theoretically this is the ...

#### 4 Logic synthesis and mapping: Placement-driven technology mapping for LUT-based FPGAs

 Joey Y. Lin, Ashok Jagannathan, Jason Cong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

**Publisher:** ACM Press


Full text available:  pdf(252.89 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study the problem of placement-driven technology mapping for table-lookup based FPGA architectures to optimize circuit performance. Early work on technology mapping for FPGAs such as Chortle-d[14] and Flowmap[3] aim to optimize the depth of the mapped solution without consideration of interconnect delay. Later works such as Flowmap-d[7], Bias-Clus[4] and EdgeMap consider interconnect delays during mapping, but do not take into consideration the effects of their mapping solution ...

**Keywords:** FPGA synthesis, logic re-synthesis, mapping

#### 5 Poster Paper Introductions: Global clustering-based performance-driven circuit partitioning

 Jason Cong, Chang Wu

April 2002 **Proceedings of the 2002 international symposium on Physical design**

**Publisher:** ACM Press

Full text available:  pdf(174.55 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we propose a new global clustering based multi-level partitioning algorithm for performance optimization. Our algorithm computes a delay minimal  $K$ -way partition first, then gradually reduces the cutsize while keeping the circuit delay by de-clustering and refinement. Our test results on a set of MCNC sequential examples show that we can reduce the delay by 30%, while increasing the cutsize by 28% on average, when compared with hMetis [5]. Our algorithm consistently outperforms ...


**Keywords:** VLSI CAD, clustering, partitioning, performance optimization, retiming

#### 6 Discovering Coherent Biclusters from Gene Expression Data Using Zero-Suppressed Binary Decision Diagrams

Sungroh Yoon, Christine Nardini, Luca Benini, Giovanni De Micheli

October 2005 **IEEE/ACM Transactions on Computational Biology and Bioinformatics (TCBB)**, Volume 2 Issue 4

**Publisher:** IEEE Computer Society Press

Full text available:  pdf(2.06 MB)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

The biclustering method can be a very useful analysis tool when some genes have multiple functions and experimental conditions are diverse in gene expression measurement. This is because the biclustering approach, in contrast to the conventional

clustering techniques, focuses on finding a subset of the genes and a subset of the experimental conditions that together exhibit coherent behavior. However, the biclustering problem is inherently intractable, and it is often computationally costly to fi ...

**Keywords:** Clustering, life and medical sciences, bioinformatics (genome or protein) databases, logic design.

## 7 Session 1A: floorplanning and partitioning: Physical planning with retiming

Jason Cong, Sung Kyu Lim

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

**Publisher:** IEEE Press

Full text available:  [pdf\(248.92 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


In this paper, we propose a unified approach to partitioning, floorplanning, and retiming for effective and efficient performance optimization. The integration enables the partitioner to exploit more realistic *geometric delay model* provided by the underlying floorplan. Simultaneous consideration of partitioning and retiming under the geometric delay model enables us to hide global interconnect latency effectively by repositioning FF along long wires. Under the proposed *geometric embedd ...*

## 8 Performance-driven multi-level clustering with application to hierarchical FPGA mapping

Jason Cong, Michail Romesis

June 2001 **Proceedings of the 38th conference on Design automation**

**Publisher:** ACM Press

Full text available:  [pdf\(216.84 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study the problem of performance-driven multi-level circuit clustering with application to hierarchical FPGA designs. We first show that the performance-driven multi-level clustering problem is NP-hard (in contrast to the fact that single-level performance-driven clustering can be solved in polynomial time optimally). Then, we present an efficient heuristic for two-level clustering for delay minimization. It can also provide area-delay trade-off by controlling the amount o ...

## 9 Invited talk: synthesis challenges for next-generation high-performance and high-density PLDs

Jason Cong, Songjie Xu

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

**Publisher:** ACM Press


Full text available:  [pdf\(2.16 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#)

## 10 Performance-driven mapping for CPLD architectures

Deming Chen, Jason Cong, Milos D. Ercegovac, Zhijun Huang

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

**Publisher:** ACM Press

Full text available:  [pdf\(265.58 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we present a performance-driven mapping algorithm, PLAmapping, for CPLD

architectures which consist of a large number of PLA-style logic cells. The primary goal of our mapping algorithm is to minimize the depth of the mapped circuit. Meanwhile, we have successfully reduced the area of the mapped circuits by applying several heuristic techniques, including threshold control of PLA fanouts and product terms, slack-time relaxation, and PLA-packing. We compare our PLAMap with a recent ...

**Keywords:** CPLD, FPGA, PLA-style logic cells, delay optimization, technology mapping

11 Performance driven multi-level and multiway partitioning with retiming



Jason Cong, Sung Kyu Lim, Chang Wu

June 2000 **Proceedings of the 37th conference on Design automation**

**Publisher:** ACM Press

Full text available: [pdf\(239.58 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper, we study the performance driven multiway circuit partitioning problem with consideration of the significant difference of local and global interconnect delay induced by the partitioning. We develop an efficient algorithm HPM (Hierarchical Performance driven Multi-level partitioning) that simultaneously considers cutsizes and delay minimization with retiming. HPM builds a multi-level cluster hierarchy and performs various refinement while gradually decomposing the clusters ...

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